IN THE SPECIFICATION:

Please amend the paragraph appearing on page 1, lines 6-27 as follows:

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The present invention is related to commonly assigned and co-pending U.S. Patent Applications [[_____ (Attorney Docket No. AUS9-2000-0569)]] 09/671,876 entitled "APPARATUS AND METHODS FOR IMPROVED DEVIRTUALIZATION OF METHOD CALLS", [[_____ (Attorney Docket No. AUS9-2000-0572)]] 09/671,973 entitled "APPARATUS AND METHOD FOR IMPLEMENTING SWITCH INSTRUCTIONS IN AN IA64 ARCHITECTURE", [[_____ (Attorney Docket No. AUS9-2000-0570)]] 09/671,770 entitled "APPARATUS AND METHOD FOR AVOIDING DEADLOCKS IN A MULTITHREADED ENVIRONMENT", [[_____ (Attorney Docket No. AUS9-2000-0584)]] 09/671,771 entitled "APPARATUS AND METHOD FOR VIRTUAL REGISTER MANAGEMENT USING PARTIAL DATA FLOW ANALYSIS FOR JUST-IN-TIME COMPILATION", [[_____ (Attorney Docket No. AUS9-2000-0585)]] 09/671,873 entitled "APPARATUS AND METHOD FOR AN ENHANCED INTEGER DIVIDE IN AN IA64 ARCHITECTURE", [[_____ (Attorney Docket No. AUS9-2000-0586)]] 09/671,874 entitled "APPARATUS AND METHOD FOR CREATING INSTRUCTION GROUPS FOR EXPLICITLY PARALLEL ARCHITECTURES", and [[_____ (Attorney Docket No. AUS9-2000-0587)]] 09/671,875 entitled "APPARATUS AND METHOD FOR CREATING INSTRUCTION BUNDLES IN AN EXPLICITLY PARALLEL ARCHITECTURE", filed on even date herewith and hereby incorporated by reference.

Please amend the paragraph appearing at page 9, line 26 to page 10, line 21 as follows:

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With reference now to **Figure 2B**, a block diagram of a data processing system in which the present invention may be implemented is illustrated. Data processing system **250** is an example of a client computer. Data processing system **250** employs a peripheral component interconnect (PCI) local bus architecture. Although the depicted example employs a PCI bus, other bus architectures such as Micro Channel and ISA may

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be used. Processor **252** and main memory **254** are connected to PCI local bus **256** through PCI Bridge **258**. PCI Bridge **258** also may include an integrated memory controller and cache memory for processor **252**. Additional connections to PCI local bus **256** may be made through direct component interconnection or through add-in boards. In the depicted example, local area network (LAN) adapter **260**, SCSI host bus adapter **262**, and expansion bus interface **264** are connected to PCI local bus **256** by direct component connection. In contrast, audio adapter **266**, graphics adapter **268**, and audio/video adapter (A/V) **269** are connected to PCI local bus [[**266**]] **256** by add-in boards inserted into expansion slots. Expansion bus interface **264** provides a connection for a keyboard and mouse adapter **270**, modem **272**, and additional memory **274**. SCSI host bus adapter **262** provides a connection for hard disk drive **276**, tape drive **278**, and CD-ROM **280** in the depicted example. Typical PCI local bus implementations will support three or four PCI expansion slots or add-in connectors.

On page 31, please amend the abstract as follows:

ABSTRACT OF THE DISCLOSURE

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APPARATUS AND METHOD FOR DETECTING AND HANDLING EXCEPTIONS

An apparatus and method are provided for detecting and handling exceptions. ~~The apparatus and method make use of predicate registers to identify whether or not an exception is pending.~~ Instructions that are executed only when there is an exception pending are qualified by a first predicate register in [[the]] a predicate register pair. Instructions that are executed only when there is no exception pending are qualified based on a second predicate register in the predicate register pair. When an exception is thrown, a determination is made as to whether or not the instruction that threw the exception is in a try block, or range, of the method that threw the exception. If not, the first predicate register predicated instruction to branch to a return stub for the method is generated. If the instruction that threw the exception is in a try block of the method, the